ABSTRACT OF THE DISCLOSURE

A half-rate clock and data recovery (CDR) circuit includes a half-rate phase detector for detecting phases of an input signal and a half-rate clock, a charge pump circuit, a low-pass filter and a voltage controlled oscillator for feeding the half-rate clock back to the half-rate phase detector. The half-rate phase detector includes a one-pulse delay circuit for generating a delay amount of one pulse such that phase comparison polarity of the half-rate phase detector provided with the one-pulse delay circuit enables use of an N type LC voltage controlled oscillator as the voltage controlled oscillator.